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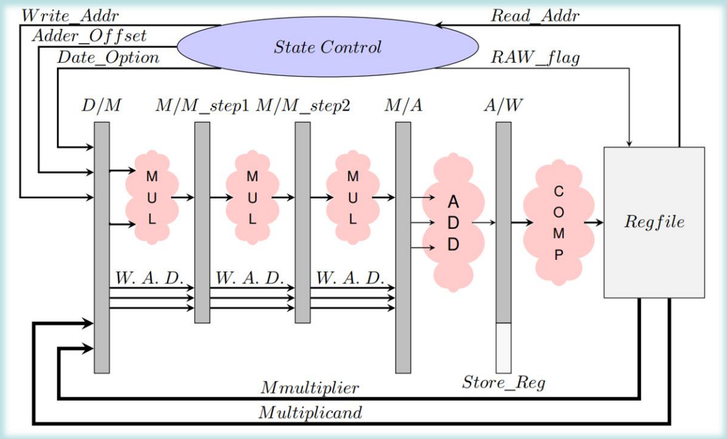
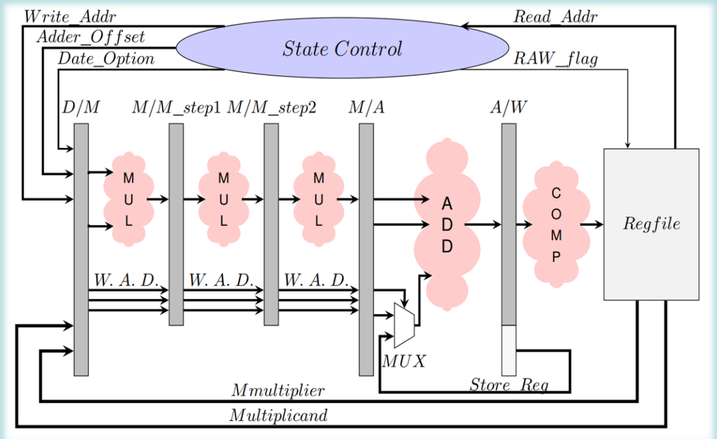
Implementation of FOC Algorithm Acceleration Circuit Based on Data Path Calculation

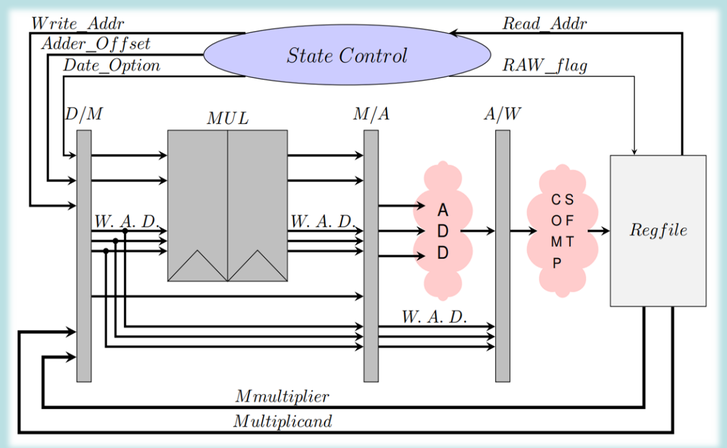
Wang Bozhi, Jiao Jiye, Xue Ziyang

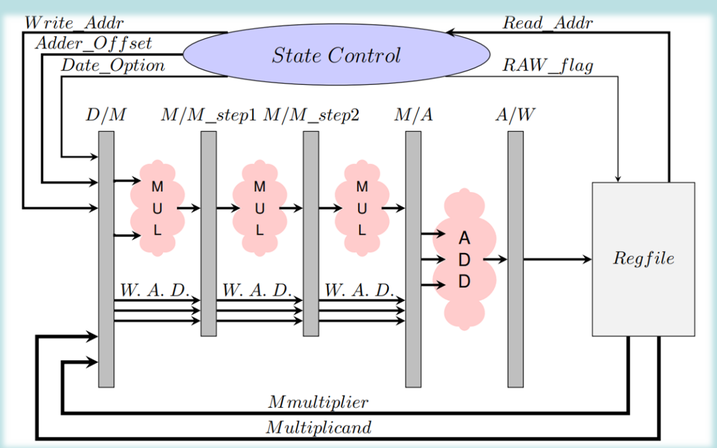
XiAn University of Posts and Telecom, China

Datapath design for FOC algorithm architecture









Matrix Multiplication, Multiply-Add-Store, Data Forwarding Multiply-Add, Additive data path

By analyzing the magnetic Field Oriented Control (FOC) algorithm, summarizing the algorithm operation steps and the use of basic units, we design multiple parallel units and the data path corresponding to the algorithm to complete the algorithm operation. This design method can effectively improve the speed of matrix operation and the calculation speed of PI control loop, and solve the problem of RAW data conflict, so that the algorithm calculation delay and pipeline waiting time can be further reduced. Finally, the Cordic module, XADC collection module, ABZ encoding module and PWM generation module are designed and combined to realize the whole circuit design. The data of the algorithm running under Simulink is collected and compared with the calculation results of the designed circuit to verify the correctness and effectiveness of the design. The circuit simulation shows that the design of a dedicated FOC algorithm architecture and data path can effectively improve the computation speed of the FOC algorithm. Experiments show that the above design can complete the computation of the FOC algorithm within 600ns (excluding the 40ns XADC sampling time).

Summary

①The parallel part of the computational steps of the FOC algorithm is extracted and analyzed as a basis for data parallelization design.

②The computational units and data since involved in the operation process of FOC algorithm are analyzed and four pathways of data operations are extracted.

③The FOC algorithm and its peripheral circuits are designed according to the data path and the circuit simulation is performed, and good design results are obtained.